Remarks/Arguments

Applicant has received and carefully reviewed the Office Action mailed October 22. 2003. Claims 1, 3-10, and 12-27 remain pending. Claims 2 and 11 have been canceled, without prejudice. Reexamination and reconsideration are respectfully requested.

In paragraph 3 of the Office Action, the Examiner rejected claims 1-3, 5-13, and 14-18 under 35 U.S.C. 102(e) as being taught by Col et al. (U.S. Patent Number 6,338,136) for the reasons set forth in the Office Action. After careful review, Applicants have amended claim 1 to recite:

> 1. (Currently Amended) A method for processing a conditional jump instruction ~~storing a digital value to memory~~ in a pipelined instruction processor~~, wherein the digital value is read from memory in response to a conditional jump instruction to determine if the condition of the conditional jump instruction is satisfied~~, the method comprising:
>
> generating at least one status bit based on [[the]] a digital value to be stored, the at least one status bit relating to a particular condition of a conditional jump instruction and specifying if the particular condition of the conditional jump instruction is satisfied or not; [[and]]
>
> storing the digital value and the at least one status bit to a memory; and
>
> in response to a conditional jump instruction, reading from the memory the digital value and the at least one status bit to determine if the condition of the conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor.

As can be seen, claim 1 recites the step of reading from memory the digital value and the at least one status bit to determine if the condition of a conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor.

The Examiner appears to be equating the status flags 561 of Col with the status bits recited in claim 1. However, the status flags 561 are clearly generated by the ALU 562 (see, for example, Col, column 12, lines 36-39). In fact, Col state:

> All that remains to be done is to resolve the conditional jump micro instruction, a task that must take place following update of the flags register 561 to reflect the status of the result of the ALU operation that is prescribed by the ALU micro instruction (Emphasis Added).

(see, Col, column 15, lines 43-48). That is, in Col, the status flags are not read from memory to determine if the condition of the conditional jump instruction is satisfied, nor does Col determine if the condition of the conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor, as recited in claim 1. For these and other reasons, claim 1 is believed to be clearly patentable over Col. For similar and other reasons, dependent claims 3-9 are also believed to be clearly patentable over Col.

Turning specifically to claim 3, which recites:

> 3. (Previously Presented) The method recited in claim 1, wherein the at least one status bit is read from memory at the same time as the digital value.

As noted above, the status flags of Col are not read from memory at the same time as the digital value. Instead, the status flags of Col and the digital value that is stored in the results register 565 (from which the status flags are generated) are stored in different locations. For these additional reasons, claim 3 is believed to be clearly patentable over Col.

Turning specifically to claim 4, which recites:

4. (Previously Presented) The method recited in claim 1, wherein the memory has one or more addressable locations, and the at least one status bit is stored at the same addressable location as the corresponding digital value.

As eluded to above, the status flags of Col are based on the operational result of the ALU, which is stored in results register 565 of Col. The status flags are stored in flags register 561. Thus, Col does not appear to store the status flags at the same addressable location as the corresponding digital value, as recited in claim 4. For these additional reasons, claim 4 is believed to be clearly patentable over Col.

In paragraph 21 of the Office Action, the Examiner states that Olsen suggests storing at least one status bits at the same addressable location as the corresponding digital value (citing Olsen, column 1, lines 36-40). However, like Col, Olsen does not appear to disclose or suggest the step of reading from memory a digital value and at least one status bit to determine if the condition of a conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor. Instead, and like Col, the status bits (i.e. status bits 15-19 of the FPSCR register 21) appear to be generated by the Floating Point Unit (i.e. ALU) (see, for example, Olsen, column 8, lines 22-26; Appendix 1, and Figure 1). Thus, claim 4 is believed to be clearly patentable over Col in view of Olsen.

Turning now to claim 10, which recites:

10. (Currently Amended) In a pipelined instruction processor that executes instructions including conditional jump instructions, one or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied, the improvement comprising:

a status bit generator for generating at least one status bit based on a digital value, the at least one status bit relating to a particular condition of a conditional jump instruction and specifying if the particular condition of the conditional jump instruction is satisfied or not; [[and]]

storing means for storing the digital value and the at least one status bit to the memory; and

conditional jump processing means, activated in response to the execution of a conditional jump instruction, the conditional jump processing means reading from the memory the digital value and the at least one status bit to determine if the condition of the conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor.

For the same reasons detailed above with respect to claim 1, as well as other reasons, claim 10 is believed to be clearly patentable over Col. For similar and other reasons, dependent claims 12-18 are also believed to be clearly patentable over Col in view of Olsen.

In paragraph 22 of the Office Action, the Examiner rejected claims 19-22 and 24-27 under 35 U.S.C. 103(a) as being unpatentable over Watson et al. in view of Col. After careful review, Applicants must respectfully disagree for a variety of reasons.

The Examiner states that Col suggests what Watson et al. is missing, including a current instruction that includes an address and a corresponding jump field, wherein the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register. The Examiner provides a number of cites to Col. However, after carefully reviewing each of the cited portions of the Col, Applicants fail to see where an instruction is shown that includes an address and a corresponding jump field, wherein the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified

addressable register. Applicants also fail to see where a number of other elements of claim 19 are disclosed or suggested by Col or Watson.

It appears that the Examiner used the exact same listing of cites to Watson to support each of the following diverse elements of claim 19: a plurality of addressable registers; logic to access a current instruction; a jump look-ahead controller; tracking logic and conflict detection logic. Likewise, it appears that the Examiner used the exact same listing of cites to Col to support each of the following diverse elements of claim 19: one or more conditional jump instructions; storing a value that includes a digital value and at least one jump status bit; wherein the current instruction includes an address and a corresponding jump field; and using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register. Applicant believes that such a rejection is improper as being unclear, and respectfully requests that the Examiner specifically point out where in Watson and/or Col each and every element of claim 19 is disclosed.

For the foregoing reasons, as well as other reasons, claim 19 is believed to be clearly patentable over Watson in view of Col. For similar and other reasons, dependent claims 20-26 are also believed to be clearly patentable over Watson in view of Col.

Turning now to claim 27, the Examiner states that Watson has taught a method for determining if a condition of a conditional jump instruction is satisfied in a pipelined instruction processor, the method comprising: (a) generating a jump look-ahead signal that is a function of the selected jump status bit read from the selected address location of the addressable memory, the identified jump status bit is accessed using the address and the jump field of the current instruction; (b) tracking the addresses of a predetermined

number of previous instructions in the pipelined instruction processor and comparing the addresses to the address of the current instruction to generate a series of jump disable signals; and (c) generating a jump early signal using the jump-look ahead signal and the series jump disable signals, the jump early signal initiates a conditional jump depending on the value of the jump disable signals.

In paragraph 35, the Examiner acknowledges that Watson has not taught (a) storing a digital value and one or more jump status bits that are based on the digital value in each of a plurality of address locations in an addressable memory; and (b) accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable memory, and the jump field identifies a selected jump status bit of the selected address location.

In paragraph 36, however, the Examiner states that Col has taught (a) storing a digital value and one or more jump status bits that are based on the digital value in each of a plurality of address locations in an addressable memory; and (b) accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable memory, and the jump field identifies a selected jump status bit of the selected address location.

As detailed above, neither Watson nor Col appear to disclose or suggest many of the elements of claim 27. The Examiner provides a number of cites to Col. However, after careful review of each of the cited portions of the Col, Applicants fail to see where, for example, an instruction is shown that includes an address and a corresponding jump field, wherein the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits

within the identified addressable register. Applicants also fail to see where a number of other elements of claim 27 are disclosed or suggested by Col or Watson. Like above, if the Examiner elects to maintain the rejection of claim 27, Applicants respectfully request that the Examiner specifically point out where in Watson and/or Col each and every element of claim 27 is disclosed. For the foregoing reasons, as well as other reasons, claim 27 is believed to be clearly patentable over Watson in view of Col.

In view of the foregoing, it is believed that all pending claims 1, 2-10 and 12-27 are now in condition for allowance. Issuance of a notice of allowance in due course is respectfully requested. If a telephone conference would be of assistance, please contact the undersigned attorney at 612-677-9050.

Respectfully submitted,

Dated: NOVEMBER 24, 2004

Brian N. Tufte, Reg. No. 38,638
CROMPTON, SEAGER & TUFTE, LLC
1221 Nicollet Avenue, Suite 800
Minneapolis, MN 55403-2402
Telephone: (612) 677-9050
Facsimile: (612) 359-9349